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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/803,083	03/08/2001	Thomas P. Glenn	G0049M	8521

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EXAMINER	
MALDONADO, JULIO J	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 04/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/803,083	GLENN ET AL.	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3 and 14-21* is/are allowed.

6)☒ Claim(s) *1 and 4-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2003/08/27*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4-7 and 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wojnarowski (U.S. 5,888,884) in view of Roberts, Jr. et al. (U.S. 5,362,681).

Wojnarowsky (Figs.1-7 and 9) teaches a method to form alignment marks (90) comprising coupling a wafer support to a first surface of a substrate; aligning a drilling device at a first intersection of a first scribe line and a second scribe line coupled to a first surface (32) of a substrate (30); drilling through said substrate (30) at said first intersection with said drilling device from said first surface (32) of said device from said first surface to a second surface (34) of said substrate to form an alignment mark (90); aligning a saw (400) with said first scribe line using said alignment mark (90), wherein said saw (400) comprises a laser saw and cutting said substrate (30) comprises cutting on the scribe lines from said second surface (34) (see Fig.7); and singulate electronic components (36) of said substrate (30), wherein said electronic components comprises integrated circuits (column 6, line 20 – column 8, line 65).

Wojnarowsky fail to teach coupling a front-side surface of a wafer to an interior surface of a transparent wafer support; optically recognizing a scribe grid coupled to

said front-side surface of said wafer, wherein said support protects the front surface of said substrate; and washing said substrate to remove contaminants generated during said cutting. However, Roberts Jr., et al. (Figs.2-5) in a related method to singularize a semiconductor wafer teach coupling a front-side surface of a wafer (32) to an interior surface of a transparent wafer support (26), wherein said support protects the front surface of said substrate and is sufficiently transparent to allow intersections in a wafer to be optically inspected through said wafer support (26); and washing said substrate to remove contaminants generated during said cutting (column 7, line 33 – column 9, line 7). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teachings of Roberts Jr. et al. and Wojnarowsky to enable the steps of coupling a front-side surface of a wafer to an interior surface of a wafer support, and furthermore because this would result in a method of separating individual dies that will provide better protection to the microstructures formed in said die (column, 3, lines 37 – 61).

3. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wojnarowski ('884) in view of Roberts, Jr. et al. ('681) as applied to claims 1, 4-7 and 9-13 above, and further in view of Summerer (U.S. 6,537,836 B2).

The combined teachings of Wojnarowski and Roberts, Jr. et al. substantially teach all aspects of the invention but fail to show shining light of an angle to said second surface of said substrate to enhance recognition of said alignment mark. However, Summerer (Fig.1) in a related method for alignment of substrates teaches shining light of an angle to a surface of a substrate (12) to detect alignment marks (column 2, lines 4 – 31). Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to use the alignment detection method as taught by Summerer to enhance recognition of an alignment mark in a second surface of a substrate in Wojnarowsky and Roberts, Jr. et al., since illuminating methods are well-known in the art to properly align a semiconductor substrate (column 1, lines 11 – 28).

Allowable Subject Matter

4. Claims 3 and 14-21 are allowed.

5. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record, Wojnarowski to U.S. 5,888,884 teaches a method to form alignment marks (90) comprising aligning a drilling device at a first intersection of a first scribe line and a second scribe line coupled to a first surface (32) of a substrate (30); drilling through said substrate (30) at said first intersection with said drilling device from said first surface (32) of said device from said first surface to a second surface (34) of said substrate to form an alignment mark (90); aligning a saw (400) with said first scribe line using said alignment mark (90), wherein said saw (400) comprises a laser saw and cutting said substrate (30) comprises cutting on the scribe lines from said second surface (34) (see Fig.7); and singulate electronic components (36) of said substrate (30), wherein said electronic components comprises integrated circuits (see Figs.1-7 and 9 and column 6, line 20 – column 8, line 65).

However, Wojnarowski fails to teach optically recognizing said first intersection through said wafer support.

Response to Arguments

6. Applicant's arguments filed 12/29/2003 have been fully considered but they are not persuasive.

Applicants argue, "...As discussed further below, Wojnarowski teaches that the front-side surface of the wafer must be processed after formation of the 'alignment holes'. Accordingly, one of skill in the art would have no motivation to apply the 'wafer support' of Roberts Jr., et al. to this front-side surface prior to the formation of the 'alignment holes' since this would defeat the ability to process the front-side surface. For at least this reason, Applicants submit that amended Claim 1 is allowable over Wojnarowski in view of Roberts Jr., et al...". This is not persuasive because it's inherent in Wojnarowski to place a support on the wafer prior to form the alignment marks. And according to Roberts Jr., et al., the use of a transparent support using a transparent support provides better protection to the microstructures formed in said die (column, 3, lines 37 – 61).

Also, in response to applicants' arguments that the combination of Wojnarowski and Roberts Jr., et al. would be inoperative because Wojnarowski further teaches processing the surfaces of the wafer, the rejected claims are open to encompass the process disclosed in Wojnarowski after using the support of Roberts Jr.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is 571-272-2800. See MPEP 203.08.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (571) 272-1855. The fax number for this group is 703-872-9306 for before final submissions, 703-872-9306 for after final submissions and the customer service number for group 2800 is (703) 306-3329. Updates can be found at http://www.uspto.gov/web/info/2800.htm.

Julio J. Maldonado
Patent Examiner
Art Unit 2823

George Fourson
Primary Examiner

Julio J. Maldonado
April 12, 2004